A 1 TO 18 GHz OUT OF PHASE COMBINER

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ABSTRACT

This paper presents the design, realization and performance of an ultra wide band 180° MMIC combiner. The circuit design is based on a simple original principle combining common-source and common-drain transistors to achieve wide band phase shifting and output matching.
Realization of the MMIC, conducted at Thomson Composant Microondes GaAs facility, has shown very good agreement between simulated and measured performance.
In the 1 to 18 GHz bandwidth, amplitude balance between the two paths is better than 0.5 dB while phase difference stays at 180° with a maximum error of 10° at 18 GHz.

INTRODUCTION

In today's electronic warfare systems, one trend is to cut down size and cost by extensive use of MMIC integration for all subfonctions involved. Such elements as magic tees, hybrid couplers, and all of the usual in phase or out of phase power dividers and combiners are unable to cover wide frequency bands such as 1-18 GHz and represent areas of about 50 mm². These passive solutions are being replaced by compact, wide band active integrated circuits [1], [2], [3] and [4]. This paper introduces an original 180° MMIC combiner which covers the 1 to 18 GHz frequency bandwidth and scales the area down by 20.

CONFIGURATION AND DESIGN

Basic principle of the circuit presented in fig. 1 is to combine two MESFETs respectively in common source and common drain configuration.

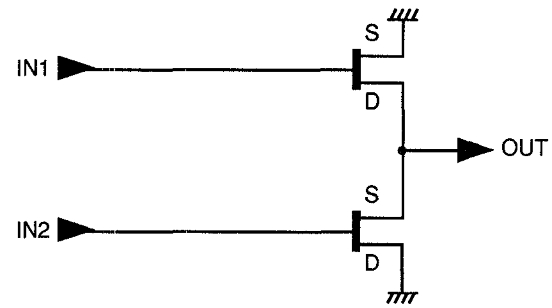

Fig. 1 : Principle of the combiner

Input signals are applied on the two gates, the output signal is being extracted between the drain of the common source transistor and the source of the common drain one.
This configuration, associating common drain and common source transistors, drives two RF output currents IDS1 and IDS2 of opposite phase.
Assuming the two MESFETs are well balanced, the two input signals are combined out of phase and at equi-amplitude. The matching and biasing networks must be designed carefully to keep the phase difference constant in the whole of the 1 to 18 GHz frequency bandwidth.
Input matching networks are indentical and consist mainly of a resistive matching network build around an L-R cell. The output impedance is nearly equal to the output impedance of the common drain MESFET alone, which can be closely enough approximated to 1/gm over the 1 to 18 GHz frequency band.
The process used to realize the circuit, exhibits a typical gm of 170 mS/mm. A 150 μm device was chosen to obtain an output transconductance of 25 mS, thus leading to an apparent output impedance close to 50 Ω without need of any further matching network.

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Each of the two transistors is biased at VDS = 3 V and VGS = 0 V. This is achieved with a single external voltage of 6 V applied at the drain of the common source MESFET. The voltage is distributed accross the two transistors and the current is flowing successively through the two devices.
The common drain MESFET is self biaised on the gate through a high value resistor placed between its source and its gate, gate voltage of the common source MESFET being set to ground. By-pass capacitors and inductors being integrated on chip, no off-chip bias circuit is needed (fig. 2).

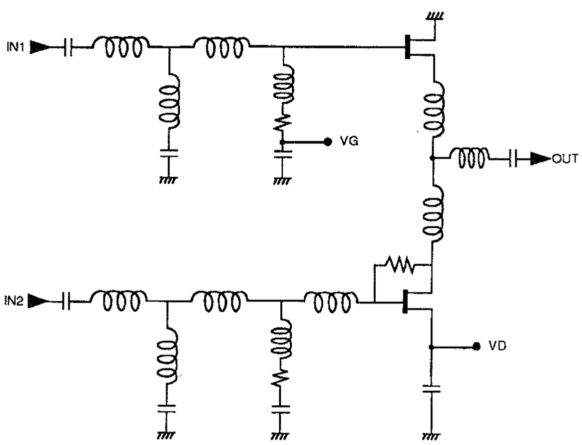

Fig. 2 : Electrical circuit

FABRICATION PROCESS

The layout was carried out with special care in order to ensure the symetry of the two paths, thus keeping the phase difference constant on all of the frequency band.
Final circuit layout is very compact, leading to a chip size of 1.5 x 1.5 mm. The active devices are two interdigitated MESFETs of 2 x 75 μm gate fingers. The fabricated chip is shown in figure 3.

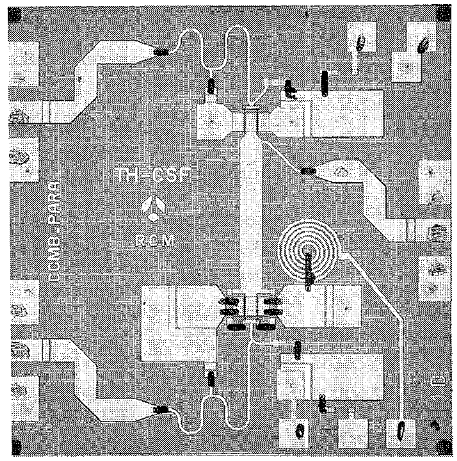

Fig. 3 : Photograph of the realized MMIC

The circuit has been processed in Thomson Composant Microondes GaAs Foundry facility using its qualified LN ∅5 process. Main characteristics of this process are Ion-implanted active layers, TiPtAu 0.5 Ebeam defined gates, implanted and TaN resistors, Si_3 N_4 overlay capacitors, spiral inductors, air bridges and via holes through 100 μm thick wafer.

PERFORMANCES

The realized MMIC has been mounted in a 380 μm thick alumina.
The measured results for this first run have shown a very tight agreement between the predicted and measured performance.
As shown in figure 4, the amplitude balance between the two inputs is within $\pm$ 0.5 dB, average absolute insertion loss being of 6.5 $\pm$ 1 dB accross the 1 to 18 frequency bandwidth.
Phase difference between the two inputs, presented in figure 5, is very close to the theoretical 180°, the maximum error of 10° being reached at 18 GHz.
Input and output (figure 6) VSWRs stay respectively below 2.5:1 and 1.9:1 in the 1-18 GHz bandwidth. Measured isolation between the two inputs is better than 20 dB.

Under the nominal bias conditions the total current is less than 20 mA, driving a DC power consumption of approximately 120 mW.
Output power, (figure 7) measured at 10 GHz, shows a 1 dB compression point at respectively 6.5 dBm and 4.4 dBm for the common-source and the common-drain paths.

CONCLUSION

This paper has described a compact, low DC power very wide band MMIC out of phase combiner using a very simple structure.
Results show good performances and excellent agreement between simulation and measurements.
We have demonstrated an out of phase combiner with ± 0,5 dB amplitude balance and 180° ± 10° phase balance in the 1-18 GHz bandwidth.

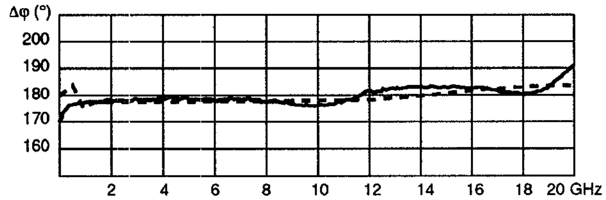

Fig. 5 : DC-20 GHz relative insertion phase performance, simulation (- - -) Versus measurements (——)

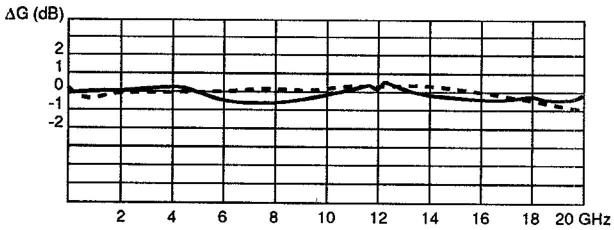

Fig. 4 a) DC-20 GHz Amplitude balance

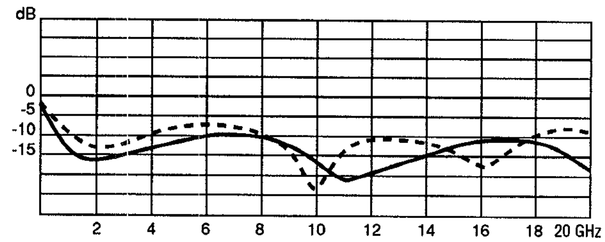

Fig. 6 : DC-20 GHz Return loss, Input (- - -) and Output

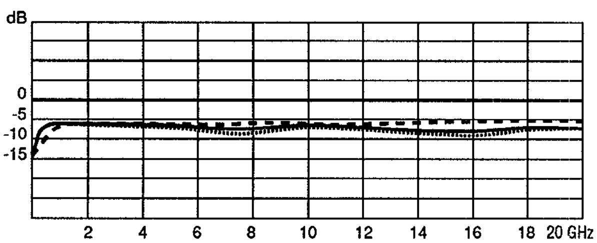

Fig. 4 b) DC-20 GHz Insertion loss performance

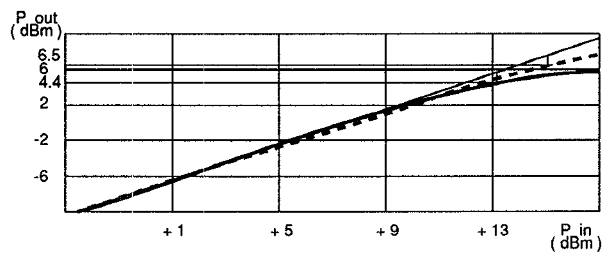

Fig. 7 : Output Power measured at F = 10 GHz

Fig. 4 : Combiner Performance, Simulation (- - -) Versus measurements (——, ····)

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